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09/944,776	08/31/2001	Andrej Kocev	15311-2310	1813

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EXAMINER	
PHAM, THOMAS K	

ART UNIT	PAPER NUMBER
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/944,776	Applicant(s) KOCEV ET AL.	
	Examiner Thomas K Pham	Art Unit 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Notice to Applicant(s)

1. Claims 13-41 of U.S. Application 09/944,776 filed on 08/31/2001 are presented for examination.

2. Applicant's amendment necessitated the new ground(s) of rejection in the following Office action.

DETAILED ACTION

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13-16, 18, 20-21, 31-32 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach et al. U.S. Patent no. 6,219,734 (hereinafter Wallach).

Regarding claims 13, 15 and 21

Wallach teaches a system for programmably allocating system resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system comprising: identifying at least one assemblies for hot swapping (col. 17 lines 33-35, "the configuration manager 1100 ... that has been hotly added"), setting criteria for transactions at the port with respect to the number of devices, and with respect to the numbers of devices at the ports, assigning resources to the ports (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers") but does not specifically teach determining the number of devices being serviced via the ports, and copying

the contents of cache memories associated with the at least one identified assemblies. However, Wallach teaches the configuration manager 500 keeps track and allocates resources for every managed adapter (col. 9 lines 18-22, "The configuration manager 500 keeps track ... allocates resources for every managed adapter") and the configuration manager 500 reprograms the newly added adapter with the old adapter's configuration (col. 12 lines 61-63, "the configuration manager 500 reprograms ... same configuration as the old adapter"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the configuration manager 500 must already determined the number of devices (resources) being service at the ports where the adapters located since originally these devices were allocated by the configuration manager 500. Furthermore, in order for the configuration manager 500 to reprogram a newly added adapter, it must already have a copy of the configuration of the old adapter in its memory prior to the replacement of the new one.

Regarding claims 14 and 16

Wallach teaches assigning system resources to the ports comprises at least one of assigning control registers to the ports, assigning direct memory access engines to the ports, assigning cache memory to the ports and assigning priorities among the transactions at the ports (col. 10 lines 58-61, "The configuration manager 500 ... adapter's configuration space registers").

Regarding claims 18 and 20

Wallach teaches the at least one identified assembly has a memory system, and the method further comprises copying the states and status of the memory systems associated with at least one identified assembly (col. 9 lines 22-25, "The registers of an adapter 310 ... the status of the adapter").

Regarding claim 31

Wallach teaches the I/O bridge comprises at least one control register, the at least one control register having a plurality of fields, and at least one field of the control register being associated with a corresponding resource, and the method further comprises writing to a selected field of the at least one control register so as to modify the assignment of resources (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers").

Regarding claim 32

Wallach teaches an Input/Output (I/O) bridge for use in a computer system having a plurality of processors, the I/O bridge comprising: a plurality of I/O ports, each I/O port configured to communicate with at least one I/O device that generates or receives transactions (col. 5 lines 1-5, "a programmable mass storage adapter ... the operational computer"); resources for use in servicing the transactions of the I/O devices (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers"); and a configuration manager 500 is responsible for configuring and arranging to assign the resources among the I/O ports in response to the number of I/O devices with which the I/O ports are communicating (col. 9 lines 15-23, "A configuration manager 500 ... during hot swap operation").

Regarding claim 41

Wallace teaches the configuration manager 500 re-assigns resources among the I/O ports dynamically while the I/O bridge continues to operate (col. 10 lines 57-61, "Once an adapter 310 ... configuration space registers").

5. Claims 17, 19, 22-25, 33 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach in view of Fung et al. U.S. Patent no. 6,243,778 (hereinafter Fung).

Regarding claims 17 and 19

Wallach teaches a system for allocating resources but does not teach determining the number and types of transactions anticipated at the ports, wherein the assignment of resources is further with respect to the numbers and types of transactions at the ports. However, Fung teaches the type and amount of data transactions anticipated by a transaction interface, in which the assignment of resource for processing data is depending on (col. 10 lines 44-49, "Depending on the type ... to be placed on the bus"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the determination of the type and amount of transactions of Fung with the system of Wallach because it would provide for determining the allocation of resources that could handle the amount and type of transactions.

Regarding claim 22

Wallach teaches a system for allocating resources but does not teach assigning a plurality of direct memory access (DMA) engines for use in processing I/O transactions. However, Fung teaches a plurality of DMA resources for use to process a large amount of data (col. 15 lines 26-31, "Every DMA channel of the ... the most efficient way possible"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the DMA resources of Fung with the system of Wallach because it would provide for processing data faster in the most efficient way possible.

Regarding claim 23

Fung teaches apportioning a selected number of DMA engines to process a given transaction at a particular I/O port (col. 15 lines 37-40, "Transaction Interface 210 ... used by their own queue").

Regarding claim 24

Fung teaches apportioning at least one DMA engine to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue").

Regarding claim 25

Wallach teaches a system for allocating resources identified as servicing multiple I/O devices (col. 4 line 64 to col. 5 line 5, "hot adding a programmable ... the I/O devices and the operational computer") and Fung teaches apportioning one DMA engine to process a given transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue").

Regarding claim 33

Wallach teaches a system for allocating resources with a configuration manager 500 but does not teach the resources comprise at least one direct memory access (DMA) engine configured to process the transactions, and the programmable logic apportions the at least one of DMA engine to process at least one transaction at a given I/O port in response to the number of I/O devices coupled to the given I/O port. However, Fung teaches at least one apportioning at least one DMA engine to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue") and apportioning a selected number of DMA engines to process a given transaction at a particular I/O port (col. 15 lines 37-40, "Transaction Interface 210 ... used by their own queue"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the DMA resources of Fung with the

system of Wallach because it would provide for processing data faster in the most efficient way possible.

Regarding claim 37

Wallach teaches a system for allocating resources with a configuration manager 500 and the I/O bridge comprising at least one cache for storing information, wherein, to hot-swap an assembly of the computer system (col. 17 lines 33-35, "the configuration manager 1100 ... that has been hotly added"), the configuration manager 500 is configured to flush the information from the at least one cache (col. 18 lines 21-27, "the FindAdapter( ) routine for an ... physical queue addresses"). Fung teaches a selected number of DMA engines to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to disable the at least one DMA engine during the selection process of which DMA engine to be utilized.

Regarding claim 38

Fung teaches the at least one cache is one of a write cache, a read cache and a translation look-aside buffer (TLB) (col. 12 lines 27-45, "Setting the "dta" bit ... has been sent or received").

Regarding claim 39

Wallach teaches does not teach the assembly is a processor. "Official Notice" is taken for both the concept and advantages of providing hot adding a processor is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include the hot adding a processor to be part of the hot adding assembly of Wallach because it would provide for adding

additional processing power to the existing computer system without interrupting the currently running processes.

Regarding claim 40

Wallach teaches the configuration manager 500 comprises at least one control register associated with each I/O port, and the at least one control register has a first field for apportioning (col. 10 lines 58-61, "The configuration manager 500 ... adapter's configuration space registers"). Fung teaches at least one apportioning at least one DMA engine to process at least one transaction at a port (col. 15 lines 32-40, "The standard procedure for the ... used by their own queue").

6. Claims 26-28 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach in view of VanDoren et al. U.S. Patent no. 6,085,294 (hereinafter VanDoren-94).

Regarding claim 26

Wallach teaches a system for allocating resources but does not teach assigning at least one miss address file (MAF) value for processing I/O transactions. However, VanDoren-94 teaches at least one miss address file (MAF) (fig. 2 element 86a). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the MAF of VanDoren-94 with the system of Wallach because it would provide for processing I/O transactions data which has not yet completed by the CPU.

Regarding claim 27

VanDoren-94 teaches assigning a plurality of miss address file (MAF) values for processing I/O transactions (col. 7 lines 38-39, "Each CPU 12a-12d ... (MAF) 86a-86d").

Regarding claim 28

Wallach and VanDoren-94 teach a system for allocating resources with at least one MAF but does not teach reducing the assigned number of MAF. However, it is obvious to one of ordinary skill in the art at the time the invention was made to reduce or increase the number of MAF in accordance with the number of CPUs used.

Regarding claim 34

Wallach teaches a system for allocating resources but does not teach the resources include a plurality of miss address file (MAF) values for use in requesting information from the computer system, and the programmable logic sets the number of available MAF values. However, VanDoren-94 teaches assigning a plurality of miss address file (MAF) values for processing I/O transactions (col. 7 lines 38-39, "Each CPU 12a-12d ... (MAF) 86a-86d"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the MAF of VanDoren-94 with the system of Wallach because it would provide for processing I/O transactions data which has not yet completed by the CPU. Furthermore, it is obvious to one of ordinary skill in the art at the time the invention was made to reduce or increase the number of MAF in accordance with the number of CPUs used.

7. Claims 29-30 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallach in view of VanDoren et al. U.S. Patent no. 6,085,276 (hereinafter VanDoren-76).

Regarding claim 29

Wallach teaches a system for allocating resources with the I/O bridge but does not teach configuring to utilize a plurality of virtual channels to communicate with at least one processors of a multiprocessor computer system, and the resources include flow control credits associated

with each of the plurality of virtual channels. However, VanDoren-76 teaches a plurality of virtual channels to communicate with the multiprocessor system, and the resources include flow control credits associated with each of the plurality of virtual channels (col. 14 line 66 to col. 15 line 5, " Virtual channels are a scheme ... among messages in the system"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the virtual channels of VanDoren-76 with the system of Wallach because it would provide for eliminating flow-dependence and resource dependence cycles among messages in the system in order to eliminating deadlock in the cache coherence protocol.

Regarding claim 30

VanDoren-76 teaches setting the number of flow control credits associated with each virtual channel (col. 20 lines 14-20, "flow control from the ... in the SMP system").

Regarding claim 35

Wallach teaches a system for allocating resources with the I/O bridge and a configuration manager 500 but does not teach the I/O bridge communicates with the computer system through a plurality of virtual channels, the resources include a plurality of flow control credits associated with the virtual channels, and the programmable logic assigns a number of flow control credits to each virtual channel. However, VanDoren-76 teaches a plurality of virtual channels to communicate with the multiprocessor system, and the resources include flow control credits associated with each of the plurality of virtual channels (col. 14 line 66 to col. 15 line 5, " Virtual channels are a scheme ... among messages in the system") and setting the number of flow control credits associated with each virtual channel (col. 20 lines 14-20, "flow control from the ... in the SMP system"). Therefore, it would have been obvious to one of ordinary skill in the art

at the time the invention was made to incorporate the virtual channels of VanDoren-76 with the system of Wallach because it would provide for eliminating flow-dependence and resource dependence cycles among messages in the system in order to eliminating deadlock in the cache coherence protocol.

Regarding claim 36

VanDoren-76 teaches the virtual channels comprise a Request channel, a Read I/O channel, and a Write I/O channel (col. 15 lines 16-28, "a Q0 channel for carrying ... from a processor to an IOP").

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (703) 305-7587 and fax number is (703) 746-8874, Monday-Thursday and every other Friday from 7:30AM- 5:00PM EST or contact Supervisor *Mr. Anil Khatri* at *(703) 305-0282.*

Any response to this office action should be mailed to: **Director of Patents and Trademarks Washington, D.C. 20231**, or **Hand-delivered** responses should be brought to **Crystal Park II, 2121 Crystal Drive Arlington, Virginia, (Receptionist located on the 4th floor),** or fax to the **official fax number (703) 872- 9306.**

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Thomas Pham
Patent Examiner

TP

March 29, 2004

GEORGE B. DAVIS
PRIMARY EXAMINER